## REMARKS

The Office Action of **November 13, 2001,** has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a One (1) Month Extension of Time* that extends the shortened statutory period for response to ***March 13, 2002.*** Accordingly, Applicant respectfully submits that this response is timely filed and fully responsive to the Office Action.

Claims 1-3, 8, 11-14, 16-19, 28, 32-34, 38-43, 52, 53, 58-60, 65, 71-73 and 75-81 were pending in this application prior to the aforementioned amendment. By the above actions, claims 1-3 and 8 are amended and new claims 100-103 added in order to place the application in better condition for allowance. Applicant respectfully submits that no issue of new matter is presented by this amendment. Accordingly, claims 1-3, 8, 11-14, 16-19, 28, 32-34, 38-43, 52, 53, 58-60, 65, 71-73, 75-81 and 100-103 are pending in this application, and are believed to be in condition for allowance for at least the reasons stated below.

## 35 U.S.C. §103 Rejection

Initially, the Office Action rejects claims 1-3, 8, 11-14, 16-19, 28, 32-34, 38-43, 52, 53, 58-60, 65, 71-73 and 75-81 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,403,772 to ***Zhang et al.*** (Hereinafter "***Zhang***") in view of U.S. Patent No. 5,233,447 to ***Kuribayashi et al.*** (Hereinafter "***Kuribayashi***") and/or U.S. Patent No. 5,173,792 to ***Matsueda***. Applicants respectfully traverse this ground for rejection for at least the reasons advanced hereinbelow. Please note that independent claims 1-3 and 8 are amended in order to more clearly recite that the TFTs of the claimed invention are intended to be used in a driver circuit or a buffer circuit for driving pixels.

The claimed invention is directed generally to circuit having the capability of flowing a large current, for example, a buffer circuit for driving pixels of an active matrix

device. As defined in claim 1, the active matrix device includes, *inter alia*, at least two transistors, a common gate wiring connected with the at least two transistors at gate electrodes of the at least two transistors, a common source wiring connected with the at least two transistors at one of source and drain of each of the at least two transistors, and a common drain wiring connected with the at least two transistors at the other of the source and drain of each of the at least two transistors. In accordance with the claimed invention, the at least two transistors are connected with each other in parallel by the connections of the common gate wiring, the common source wiring and the common drain wiring with the at least two transistors.

Applicant respectfully contends that the claimed invention defines subject matter which is clearly patentably distinct over the prior art of record. More particularly, Applicant respectfully contends that the ***Zhang*** patent, either alone or in combination with the ***Kuribayashi*** and/or ***Matsueda*** patents, fails to expressly teach or inherently suggest each and every claim limitation of the present invention necessary to support a *prima facie* case of obviousness under §103.

In the Office Action, the Examiner finds that ***Zhang*** allegedly discloses an active matrix type LC display device substantially as claimed in the present invention. The Examiner concedes, however, that ***Zhang*** fails to disclose (1) a buffer circuit in the driver circuit and (2) a peripheral driver circuit comprising at least two TFTs connected in parallel. ***Kuribayashi*** was cited in order to cure the first deficiency since it allegedly discloses a display device including a buffer circuit. In order to cure the second deficiency, ***Matsueda*** was cited since it allegedly discloses an active matrix type LC display device comprising at least two TFTs (100A and 100B) which are connected in parallel on the surface of an insulating layer (110).

As illustrated in FIG. 7, the TFTs (100A and 100B) disclosed in ***Matsueda*** are provided at respective pixels of the display device, and are not related to a buffer circuit

for use in a driver circuit of a display device. Accordingly, there is a lack of motivation to combine the respective teachings of ***Zhang***, ***Kuribayashi*** and ***Matsueda*** to produce the claimed invention. Regardless of the type of disclosure, the prior art must provide some motivation to one of ordinary skill in the art to make the claimed invention in order to support a conclusion of obviousness. *In re Vaeck,* 942 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991). Applicant respectfully contends that the motivation to combine the prior art references supplied by the Examiner came as the result of impermissible hindsight reconstruction of the claimed invention. It is a well-established rule that obviousness cannot be predicated by hindsight combination to produce the claimed invention. *In re Gorman*, 933 F.2d 982, 986, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991).

For instance, in an effort to construct an integrated active matrix type display device, it is desirable to form not only the pixel region but also the peripheral circuitry on a single substrate. In such cases, the TFTs which are arranged on the peripheral circuitry should have the ability to manage large currents in order to drive the many thousands pixel electrodes. Operating at such large currents, however, produces excess heat and degradation of characteristics in the active matrix type display device. Consequently, a buffer amplifier (i.e., a power conversion circuit which has a low output impedance) comprising TFTs in the peripheral circuitry is provided to manage the large currents. However, in order to construct a TFT which can be used in a buffer amplifier, it is necessary for the channel-forming region of the TFT to have a width of several tens of micrometers or more.

Accordingly, in order to obviate the above-noted problems in the related art, the Applicants' have provided an active matrix-type display device comprising at least two transistors provided on an insulating surface in a buffer circuit of a driver circuit, whereby channel-forming regions of the at least two transistors are separately provided in at least two separate islands respectively. See, FIG. 3. Such a construction produces an

active matrix-type display device which yields certain non-obvious benefits such as high voltage resistance and high speed performance that does not result in the degradation or variation of characteristics of the active matrix-type display device.

***Matsueda*** is not concerned with these problems, as evidenced by ***Matsueda's*** silence concerning the use of a driver circuit. Accordingly, ***Matsueda's*** lack of recognition of the problems solved by the Applicants' is further indicative of the nonobviousness of the claimed invention. Inasmuch as the ***Zhang***, ***Kuribayashi*** and ***Matsueda*** patents provide no apparent motivation to combine their respective teachings, one of ordinary skill in the art would not look to them in order produce the claimed invention. Accordingly, Applicant respectfully requests that the §103(a) rejection of the pending claims be reconsidered and withdrawn in view thereof.

## Conclusion

Accordingly, Applicant submits that the pending claims are in proper condition for allowance and consideration and withdrawal of the pending rejections is requested. If the Examiner believes further discussions with applicant's representative would be beneficial in this case, he is invited to contact the undersigned.

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285
NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

EJR/TAV

MARKED UP COPY OF AMENDED CLAIMS

1. (Thrice Amended) An active matrix type display device comprising:

a plurality of pixels arranged in matrix form over a substrate;

a driver circuit for driving the plurality of pixels over said substrate, said driver circuit including at least one buffer circuit;

at least two transistors [provided on an insulating surface in a] in said at least one buffer circuit [in said active matrix type display device];

a common gate wiring [provided over said insulating surface and] connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring [provided over said insulating surface and] connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring [provided over said insulating surface and] connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively[, each of said channel-forming regions containing carbon and nitrogen at a concentration of $5 \times 10^{18}$ $cm^{-3}$ or less, respectively, and containing oxygen at a concentration of $5 \times 10^{19}$ $cm^{-3}$ or less].

2. (Thrice Amended) An active matrix type display device comprising:

a plurality of pixels arranged in matrix form over a substrate;

a driver circuit for driving the plurality of pixels over said substrate;

at least two transistors [provided on an insulating surface in a] in said driver circuit [in said active matrix type display device];

a common gate wiring [provided over said insulating surface and] connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring [provided over said insulating surface and] connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring [provided over said insulating surface and] connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively[, each of said channel-forming regions containing carbon and nitrogen at a concentration of $5 \times 10^{18}$ $cm^{-3}$ or less, respectively, and containing oxygen at a concentration of $5 \times 10^{19}$ $cm^{-3}$ or less].

3. (Thrice Amended) An active matrix type display device comprising:

a plurality of pixels arranged in matrix form over a substrate;

a driver circuit for driving the plurality of pixels over said substrate, said driver circuit including at least one buffer circuit;

at least two transistors [provided on an insulating surface in a] in said at least one buffer circuit [in said active matrix type display device];

a common gate wiring [provided over said insulating surface and] connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring [provided over said insulating surface and] connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring [provided over said insulating surface and] connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively[, each of said channel-forming regions containing carbon and nitrogen at a concentration of $5 \times 10^{18}$ $cm^{-3}$ or less, respectively, and containing oxygen at a concentration of $5 \times 10^{19}$ $cm^{-3}$ or less,] and each of said channel-forming regions not having linear defects or surface defects.

8. (Thrice Amended) An active matrix type display device comprising:

a plurality of pixels arranged in matrix form over a substrate;

a driver circuit for driving the plurality of pixels over said substrate;

at least two transistors [provided on an insulating surface in a] in said driver circuit in said active matrix type display device;

a common gate wiring [provided over said insulating surface and] connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring [provided over said insulating surface and] connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring [provided over said insulating surface and] connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively[, each of said channel-forming regions containing carbon and nitrogen at a concentration of 5 x $10^{18}$ $cm^{-3}$ or less, respectively, and containing oxygen at a concentration of 5 x $10^{19}$ $cm^{-3}$ or less,] and each of said channel-forming regions not having linear defects or surface defects.